LXT901

Universal Ethernet Interface Adapter (Internal MAU) with Integrated 10BASE-T MAU, EnDec, AUI and Filters

General Description

The LXT901 Universal Ethernet Interface Adapter is designed for IEEE 802.3 physical layer applications. It provides all the active circuitry to interface most standard 802.3 controllers to either the 10BASE-T media or Attachment Unit Interface (AUI). In addition to standard 10 Mbps Ethernet, the LXT901 also supports full-duplex operation at 20 Mbps.

LXT901 functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing and reversed polarity detection/correction. The LXT901 can be used to drive either the AUI drop cable or the 10BASE-T twisted-pair cable with only a simple isolation transformer. Integrated filters simplify the design work required for FCC compliant EMI performance. Selectable termination impedance allows the LXT901 to be used with either shielded or unshielded twisted-pair cable.

The LXT901 is fabricated with an advanced CMOS process and requires only a single 5 volt power supply.

Applications

- Laptop/Palmtop portables (PCMCIA compatibles)
- Computer/workstation 10BASE-T LAN adapter boards

Features

Functional Features

- Integrated Filters - Simplifies FCC Compliance
- Integrated Manchester Encoder/Decoder
- 10BASE-T compliant Transceiver
- AUI Transceiver
- Supports Standard and Full-Duplex Ethernet

Convenience Features

- Automatic/Manual AUI/RJ45 Selection
- Automatic Polarity Correction
- Programmable Impedance Driver
- Power Down Mode and four loopback modes
- Available in 64-pin TQFP and 44-pin PLCC packages

Diagnostic Features

- Four LED Drivers
- AUI/RJ45 Loopback
- Remote Signaling of Link Down and Jabber conditions

LXT901 Block Diagram

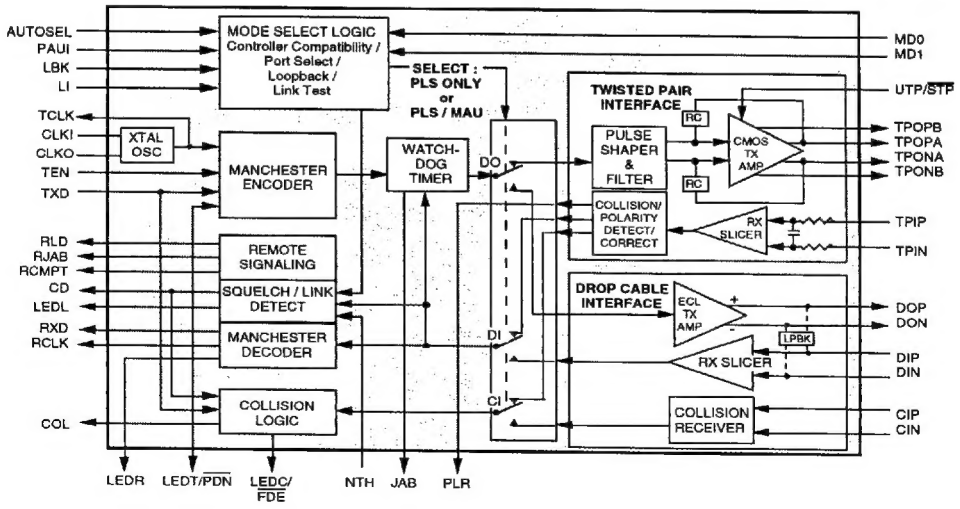

Figure 1: LXT901 Pin Assignments

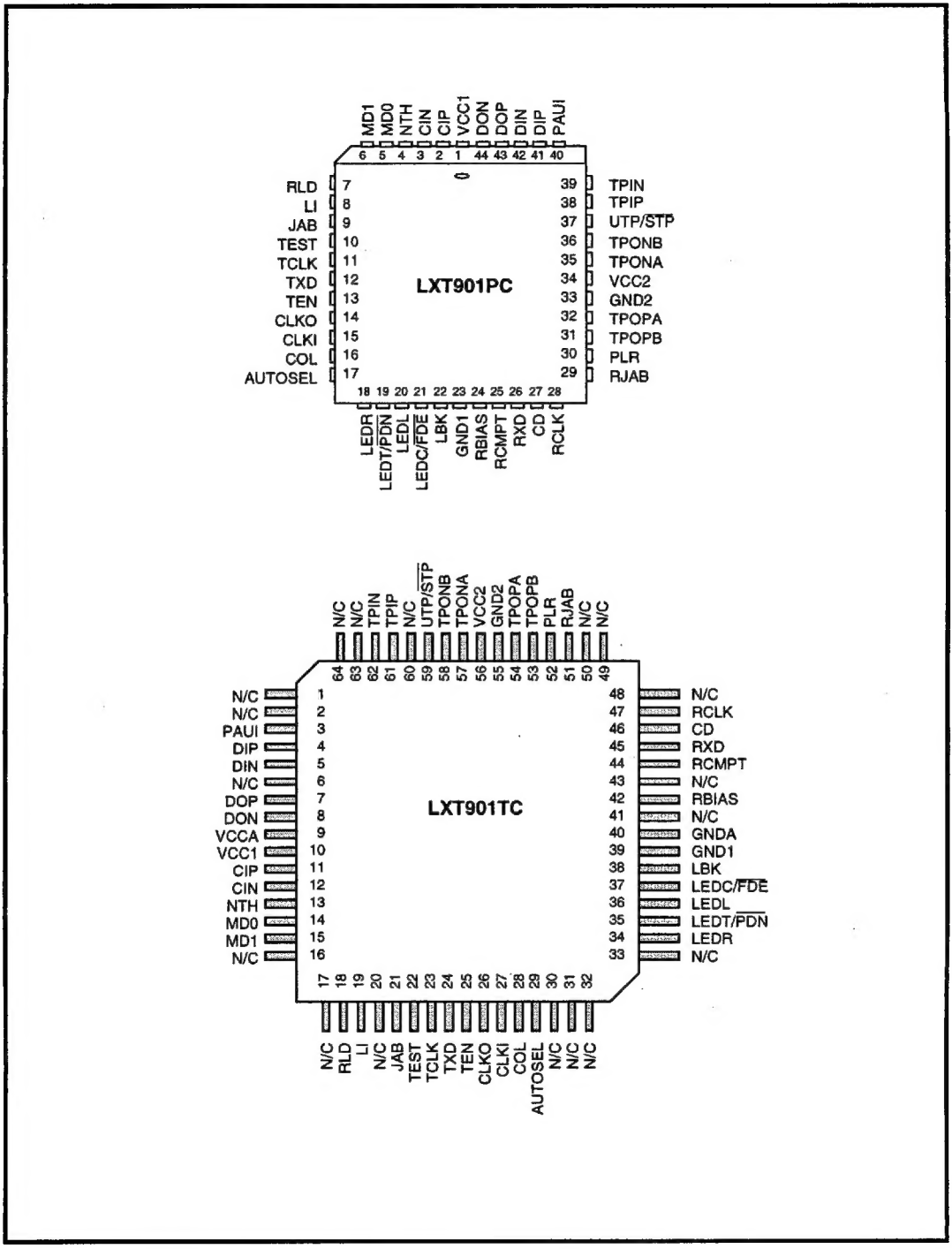

Table 1: LXT901 Pin Descriptions

PLCC	TQFP	Sym	I/O	Name	Description
1 34 –	10 56 9	VCC 1 VCC 2 VCCA	I I I	Power Inputs 1, 2 and A (TQFP only)	+ 5 volt power supply inputs.
2 3	11 12	CIP CIN	I I	AUI Collision Pair	Differential input pair connected to the AUI transceiver CI circuit. The input is collision signaling or SQE.
4	13	NTH	I	Normal Threshold	When NTH is High, the normal TP squelch threshold is in effect. When NTH is Low, the normal TP squelch threshold is reduced by 4.5 dB.
5 6	14 15	MD0 MD1	I I	Mode Select 0 Mode Select 1	Mode select pins determine controller compatibility mode in accordance with Table 2.
7	18	RLD	O	Remote Link Down	Output goes high to signal to the controller that the remote port is in link down condition.
8	19	LI	I	Link Test Enable	Controls Link Integrity Test; enabled when High, disabled when Low.
9	21	JAB	O	Jabber Indicator	Output goes high to indicate Jabber state.
10	22	TEST	I	Test	This pin must be tied High.
11	23	TCLK	O	Transmit Clock	A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.
12	24	TXD	I	Transmit Data	Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
13	25	TEN	I	Transmit Enable	Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Test Specifications for details).
14 15	26 27	CLKO CLKI	O I	Crystal Oscillator	A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	28	COL	O	Collision Detect	Output which drives the collision detect input of the controller.
17	29	AUTO SEL	I	Automatic Port Select	When High, automatic port selection is enabled (the 901 defaults to the AUI port only if TP link integrity = Fail). When Low, manual port selection is enabled (the PAUI pin determines the active port).
18	34	LEDR	O	Receive LED	Open drain driver for the receive indicator LED. Output is pulled Low during receive.
19	35	LEDT/ $\overline{\text{PDN}}$	O I	Transmit LED/ Power Down	Open drain driver for the transmit indicator. Output is pulled Low during transmit. If externally tied Low, the LXT901 goes to power down state.
20	36	LEDL	O I	Link LED	Open drain driver for link integrity indicator. Output is pulled Low during link test pass. If externally tied Low, internal circuitry is forced to "Link Pass" state and 901 will continue to transmit link test pulses.
21	37	LEDC/ $\overline{\text{FDE}}$	O I	Collision LED	Open drain driver for the collision indicator pulls Low during collision. If externally tied Low, the LXT901 disables the internal TP loopback and collision detect circuits for full-duplex operation or external TP loopback.

Table 1: Pin Descriptions - continued

PLCC	TQFP	Sym	I/O	Name	Description
22	38	LBK	I	Loopback	Enables internal loopback mode. Refer to Test Specifications for details.
23 33 –	39 55 40	GND1 GND2 GNDA	– – –	Ground Returns 1, 2 and A (TQFP only)	Grounds.
24	42	RBIAS	I	Bias Control	A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
25	44	RCMPT	O	Remote Compatibility	Output goes High to signal the controller that the remote port is compatible with the LXT901 remote signaling features.
26	45	RXD	O	Receive Data	Output signal connected directly to the receive data input of the controller.
27	46	CD	O	Carrier Detect	An output to notify the controller of activity on the network.
28	47	RCLK	O	Receive Clock	A recovered 10 MHz clock which is synchronous to the received data and connected to the controller receive clock input.
29	51	RJAB	O	Remote Jabber	Output goes High to indicate that the remote port is in Jabber condition.
30	52	PLR	O	Polarity Reverse	Output goes High to indicate reversed polarity at the TP input.
31 36 32 35	53 58 54 57	TPOPB TPONB TPOPA TPONA	O O O O	Twisted-Pair Transmit Pairs A & B	Two differential driver pair outputs (A and B) to the twisted-pair cable. The outputs are pre-equalized; no external filters are required. Two pairs are used to provide compatibility with both 100 Ω load cable and 150 Ω load cable.
37	59	UTP/ $\overline{\text{STP}}$	I	UTP / $\overline{\text{STP}}$ Select	When UTP is Low, 150 Ω termination for shielded TP is selected. When UTP is High, 100 Ω termination for unshielded TP is selected.
38 39	61 62	TPIP TPIN	I I	Twisted-Pair Receive Pair	A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip.
40	3	PAUI	I	Port/AUI Select	In Manual Port Select mode (AUTOSEL Low), PAUI selects the active port. When PAUI is High, the AUI port is selected. When PAUI is Low, the TP port is selected. In Auto Port Select mode, PAUI must be tied to ground.
41 42	4 5	DIP DIN	I I	AUI Receive Pair	Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	7 8	DOP DON	O O	AUI Transmit Pair	A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.

FUNCTIONAL DESCRIPTION

NOTE
This information is for design aid only.

The LXT901 Universal Ethernet Interface Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as a PLS-Only device (for use with 10BASE-2 or 10BASE-5 coaxial cable networks) or as an Integrated PLS/MAU (for use with 10BASE-T twisted-pair networks). In addition to standard 10 Mbps operation, the LXT901 also supports full-duplex 20 Mbps operation.

The LXT901 interfaces a back end controller to either an AUI drop cable or a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the LXT901 contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The LXT901 Transmit function refers to data transmitted by the back end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/MAU mode). The LXT901 Receive function refers to data received by the back end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the LXT901 performs all required MAU functions defined by the IEEE 802.3 10BASE–T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback. In the PLS-Only mode, the LXT901 receives incoming signals from the AUI DI circuit with ± 18 ns of jitter and drives the AUI DO circuit.

CONTROLLER COMPATIBILITY MODES

The LXT901 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Intel, Fujitsu, National Semiconductor, Seeq and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins (MD0 and MD1) determine Controller compatibility modes as listed in Table 2. Refer to Test Specifications for a complete set of timing diagrams for each mode.

TRANSMIT FUNCTION

The LXT901 receives NRZ data from the controller at the TXD input as shown in the first diagram, and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure 2. The TPO output is pre-distorted and prefiltered to meet the 10BASE-T jitter template. **An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance.** During idle periods, the LXT901 transmits link integrity test pulses on the TPO circuit (if LI is enabled and integrated PLS/ MAU mode is selected). The UTP pin controls LXT901 termination impedance.

When UTP/$\overline{\text{STP}}$ is Low, the LXT901 is set for shielded TP (150 Ω). When UTP/$\overline{\text{STP}}$ is High, the LXT901 is set for unshielded TP (100 Ω).

Figure 2: LXT901 TPO Output Waveform

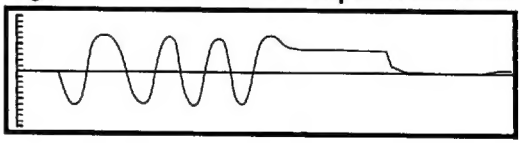

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Table 2: Controller Compatibility Mode Options

Controller Mode:	Setting: MD1	MD0
Mode 1 - For Advanced Micro Devices AM7990 or compatible controllers	Low	Low
Mode 2 - For Intel 82596 or compatible controllers	Low	High
Mode 3 - For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005)[1]	High	Low
Mode 4 - For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	High	High

1. SEEQ controllers require inverters on CLKI, LBK, RCLK and COL.

JABBER CONTROL FUNCTION

Figure 3 is a state diagram of the LXT901 Jabber control function. The LXT901 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JAB pin. Once the LXT901 is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

SQE FUNCTION

In the integrated PLS/MAU mode, the LXT901 supports the signal quality error (SQE) function as shown in Figure 4. After every successful transmission on the 10BASE-T network, the 901 transmits the SQE signal for 10BT±5BT over the internal CI circuit which is indicated on the COL pin of the device. When using the 10BASE-2 port of the 901, the SQE function is determined by the external MAU attached.

RECEIVE FUNCTION

The LXT901 receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT901 receive function enters the idle state. If the polarity of the TPI circuit is reversed, LXT901 detects the polarity reverse and reports it via the PLR output. The LXT901 automatically corrects reversed polarity.

Figure 3: Jabber Control Function

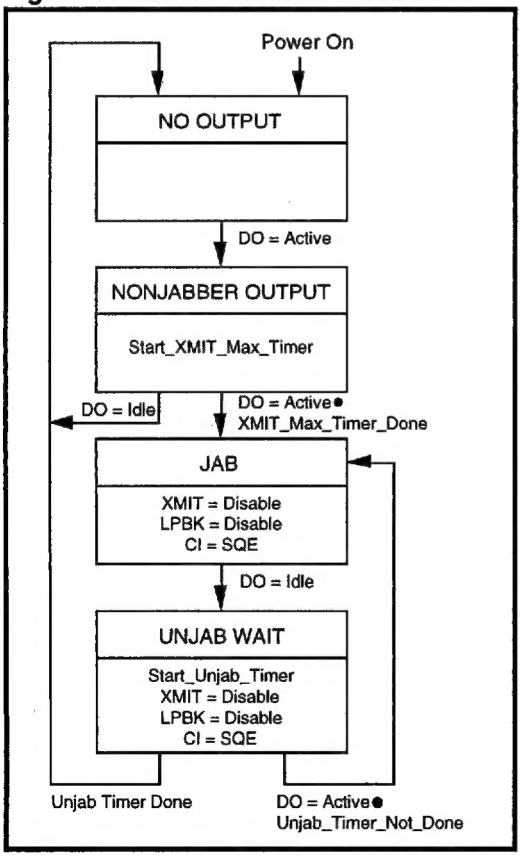
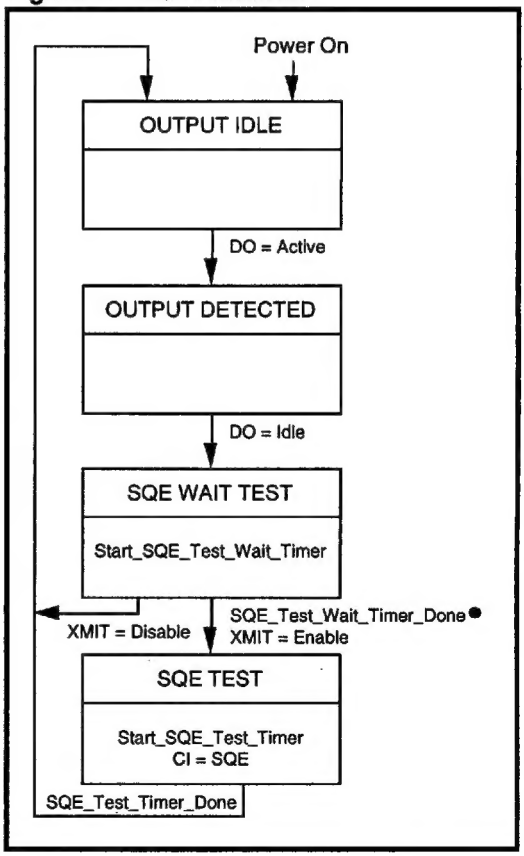


Figure 4: SQE Function



POLARITY REVERSE FUNCTION

The LXT901 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the LXT901 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.). Polarity correction is always enabled.

COLLISION DETECTION FUNCTION

The collision detection function operates on the twisted-pair side of the interface. For standard (half-duplex) 10BASE-T operation, a collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT901 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 5 is a state diagram of the LXT901 collision detection function. Refer to Test Specifications for collision detection and COL/CI output timing (NOTE: For full-duplex operation, the collision detection circuitry must be disabled.)

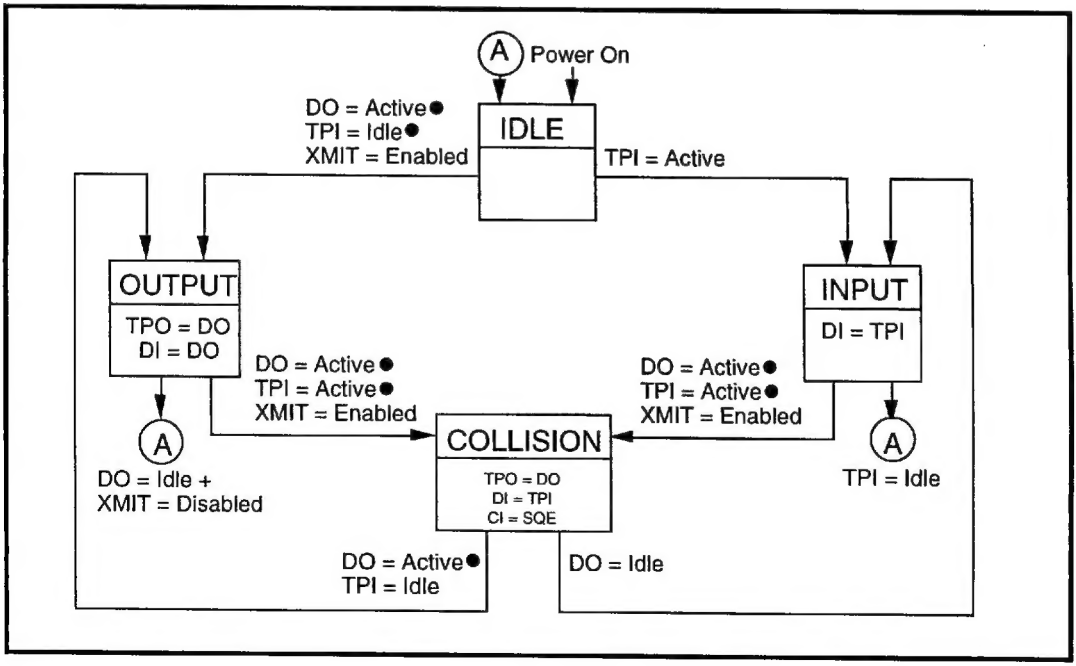
LOOPBACK FUNCTION

The LXT901 provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT901 from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This "normal" loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Normal loopback is also disabled during link fail and jabber states.

The LXT901 also provides three additional loopback functions. An external loopback mode, useful for system-level testing, is controlled by pin 21 (LEDC/$\overline{\text{FDE}}$). When LEDC/$\overline{\text{FDE}}$ is tied Low, the LXT901 disables the collision detection and internal loopback circuits, to allow external loopback.

"Forced" TP loopback is controlled by pin 22 (LBK). When the TP port is selected and LBK is High, TP loopback is "forced", overriding collisions on the TP circuit. When LBK is Low, normal loopback is in effect.

Figure 5: Collision Detection Function

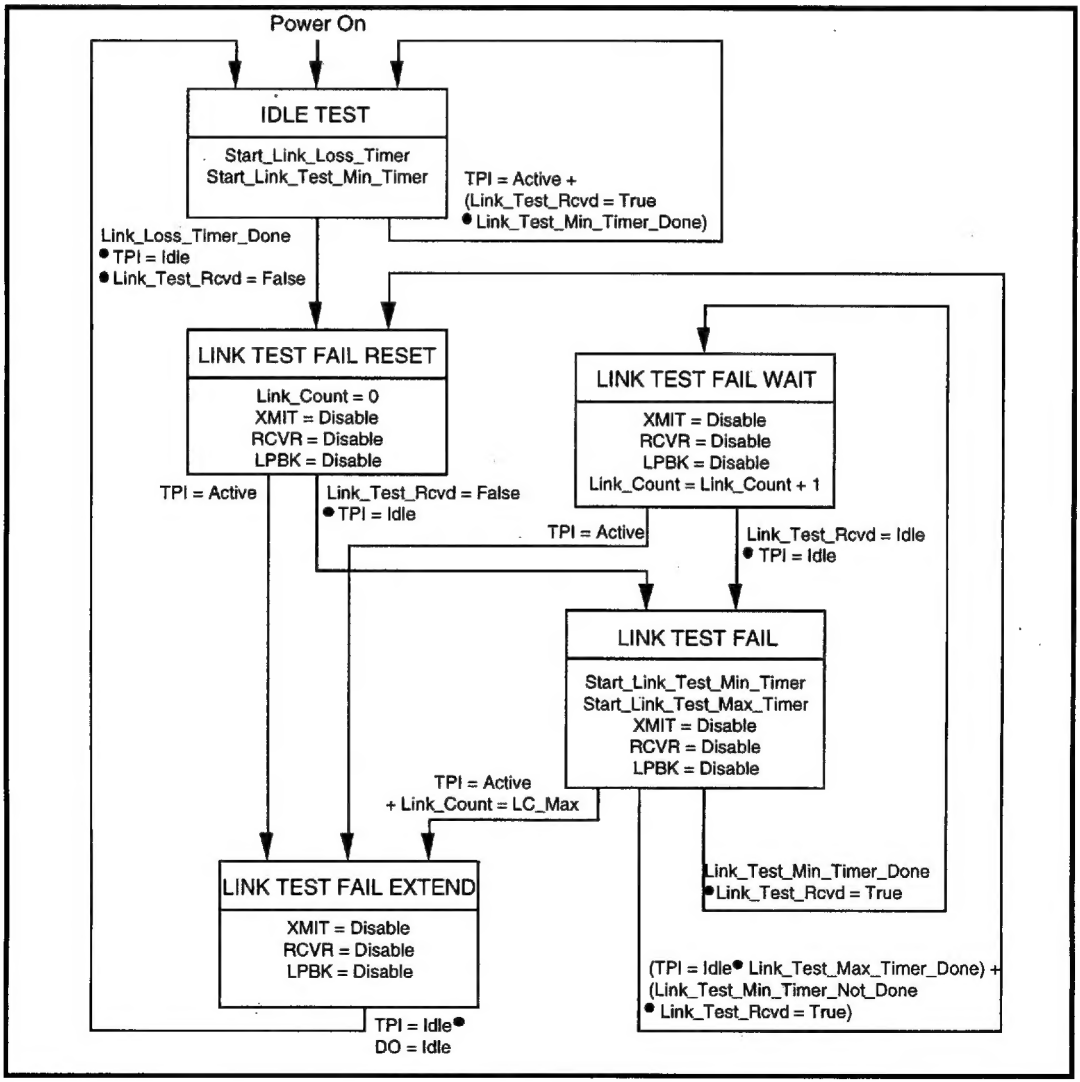


AUI loopback is also controlled by the LBK pin. When the AUI port is selected and LBK is High, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK is Low, no AUI loopback occurs.

LINK INTEGRITY TEST

Figure 6 is a state diagram of the LXT901 Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 8 (LI) is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT901 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT901 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

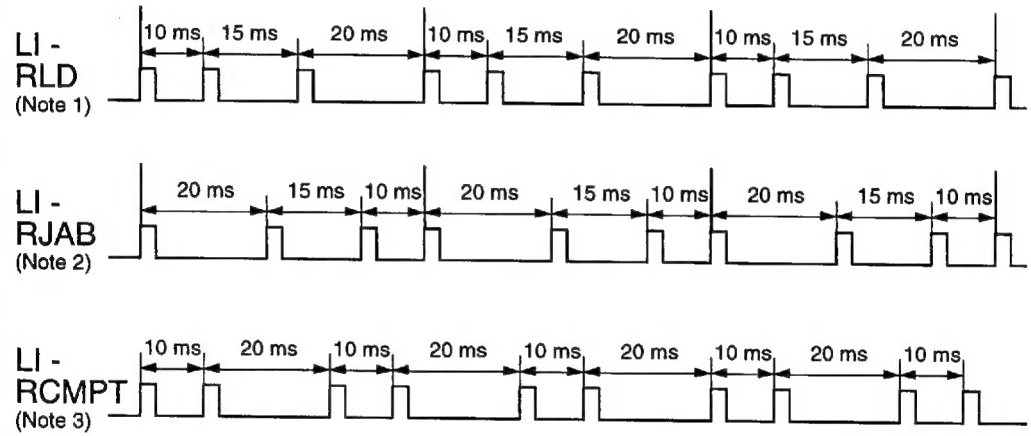
Figure 6: Link Integrity Test Function



REMOTE SIGNALING

The LXT901 transmits standard link pulses which meet the 10BASE-T specification. However, the LXT901 encodes additional status information into the link pulse by varying the link pulse timing. This is referred to as remote signaling. Using alternate pulse intervals, the LXT901 can signal three local conditions: link down, jabber, and remote signaling compatibility. Figure 7 shows the interval variations used to signal local status to the other end of the line. The LXT901 also recognizes these alternate pulse intervals when received from a remote unit. Remote status conditions are reported to the controller over the RLD, RJAB and RCMPT output pins.

Figure 7: Remote Signaling Link Integrity Pulse Timing



NOTES

1. For Remote Link Down (RLD) signaling, the interval between LI pulses increments from 10 ms to 15 ms to 20 ms, and then the cycle starts over.
2. For Remote Jabber (RJAB) signaling, the interval between LI pulses decrements from 20 ms to 15 ms to 10 ms, and then the cycle starts over.
3. For Remote Compatibility (RCMPT) signaling, the interval between LI pulses continually switches between 10 ms and 20 ms.

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APPLICATION INFORMATION

NOTE
This information is for design aid only.

Figures 8 through 15 show typical LXT901 applications.

AUTO PORT SELECT WITH EXTERNAL LOOPBACK CONTROL (FIGURE 8)

Figure 8 is a typical LXT901 application. The diagram is arranged to group similar pins together; it does not represent the actual LXT901 pinout. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

Programmable option pins are grouped center left. The PAUI pin is tied Low and all other option pins are tied High. This set-up selects the following options:

- Automatic Port Selection (PAUI Low and AUTOSEL High)
- Normal Receive Threshold (NTH High)
- Mode 4 (compatible with National NS8390 controllers) (MD0 High, MD1 High)
- 100 Ω termination for unshielded TP cable (UTP/$\overline{\text{STP}}$ High)
- Link Testing Enabled (LI High)

Status outputs are grouped at lower left. Local status outputs drive LED indicators and remote status indicators are available as required.

Power and ground pins are shown at the bottom of the diagram. A single power supply is used for both VCC1 and VCC2 with a decoupling capacitor installed between the power and ground busses.

The TP and AUI interfaces are shown at upper and lower right, respectively. Impedance matching resistors are installed in each I/O pair but no external filters are required. Suitable transformers are listed in notes 2 and 3.

DUAL NETWORK SUPPORT - 10BASE T AND TOKEN RING (FIGURE 9)

Figure 9 shows the LXT901 with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both High). When used with the 380C26, both the LXT901 and a TMS38054 Token Ring transceiver can be tied to a single RJ45 allowing dual network support from a single connector. The LXT901 AUI port is not used.

MANUAL PORT SELECT WITH LINK TEST FUNCTION (FIGURES 10 AND 11)

With MD0 Low and MD1 tied High, the LXT901 logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 and MB86960, and SEEQ 8005 controllers). Figure 10 shows the setup for Fujitsu controllers. Figure 11 shows the four inverters required to interface with the SEEQ 8005 controller. As in Figure 8, both these Mode 3 applications show the LI pin tied High, enabling Link Testing; and the UTP/$\overline{\text{STP}}$ and NTH pins are both tied High, selecting the standard receiver threshold and 100 Ω termination for unshielded TP cable. However, in these applications AUTOSEL is tied Low, allowing external port selection through the PAUI pin. The remote status outputs are inverted to drive LED indicators.

150 Ω SHIELDED TWISTED-PAIR ONLY (FIGURE 12)

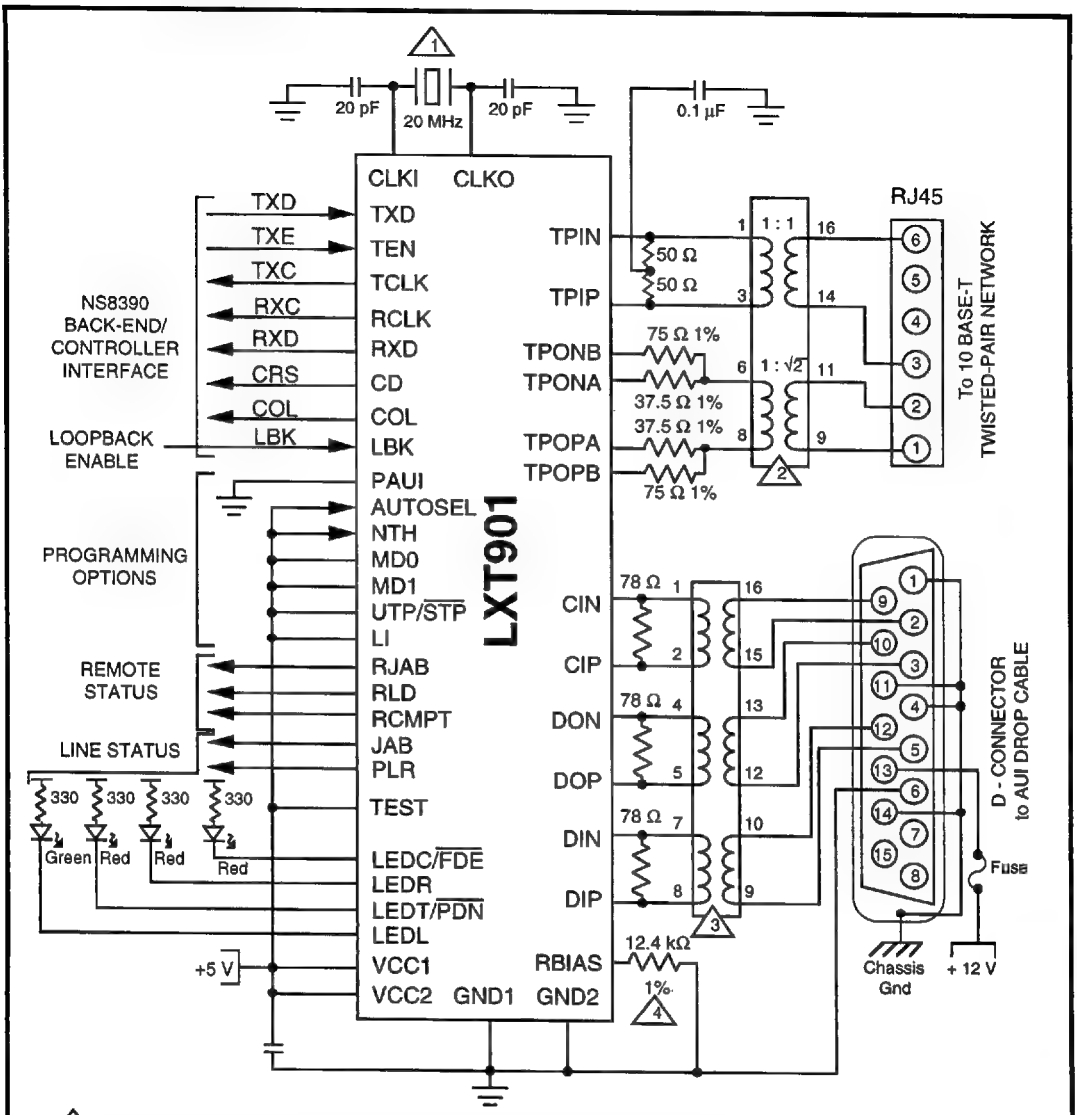
Figure 12 shows the LXT901 in a typical twisted-pair only application. The DTE is connected to a 10BASE-T network through the twisted-pair RJ45 connector. (The AUI port is not used.) With MD0 tied High and MD1 Low, the LXT901 logic and framing are set to Mode 2 (compatible with Intel 82596 controllers).

A 20 MHz system clock input at CLKI is used in place of the crystal oscillator. (CLKO is left open.) The LI pin externally controls the link test function. The UTP/$\overline{\text{STP}}$ and NTH pins are both tied Low, selecting the reduced receiver threshold and 150 Ω termination for shielded TP cable. The switch at LEDT/$\overline{\text{PDN}}$ manually controls the power down mode.

THREE MEDIA APPLICATION (FIGURE 13)

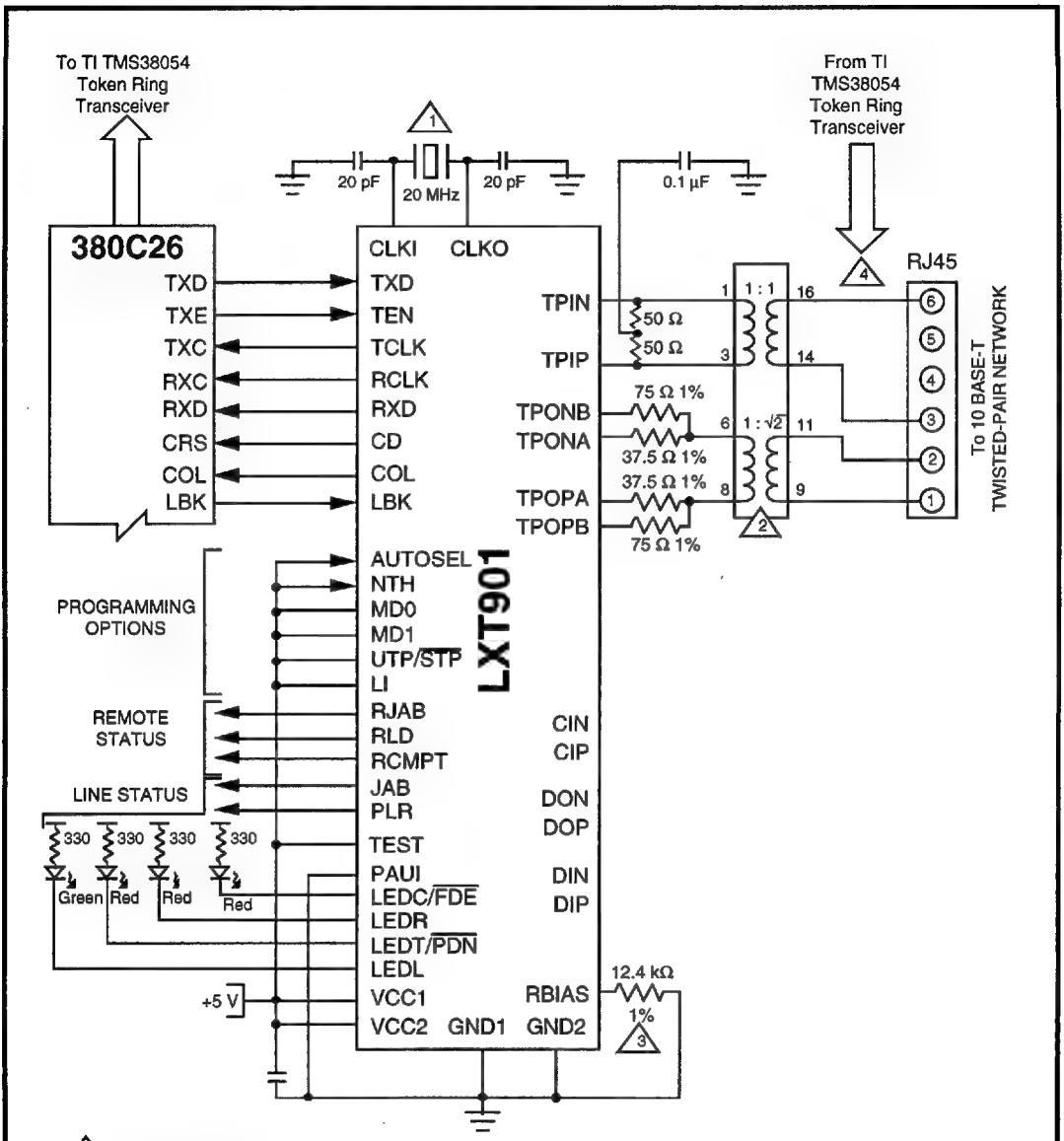
Like Figure 12, Figure 13 shows the LXT901 in Mode 2 (compatible with Intel 82596 controllers) with the same options and twisted-pair interface. However, Figure 13 adds a pair of connections to the AUI port which was not used in Figure 12. Two transformers are used to couple the AUI port to either a D-connector or a BNC connector. (A DP8392 coax transceiver with PM6044 power supply are required to drive the thin coax network through the BNC.)

Figure 8: LAN Adapter Board - Auto Port Select with External LPBK Control



1. Suitable crystals include the MTRON MP-1 and MP-2.
2. Suitable TP transformers include the Fil-Mag 23Z128, and 23Z128SM; Valor PT4069 and ST7011; Belfuse S553-0716 and A553-0716; and Halo Electronics TD42-2006Q and TG42-2006WH1.
3. Suitable AUI transformers include the Fil-Mag 23Z90 and 23Z90SM; Valor LT6030 and ST7030; and Halo Electronics TD01-0756K and TG01-0756W.
4. Bias resistor RBIAS should be located close to the pin and isolated from other signals.

Figure 9: LXT901/380C26 Interface for Dual Network Support of 10BASE-T and Token Ring



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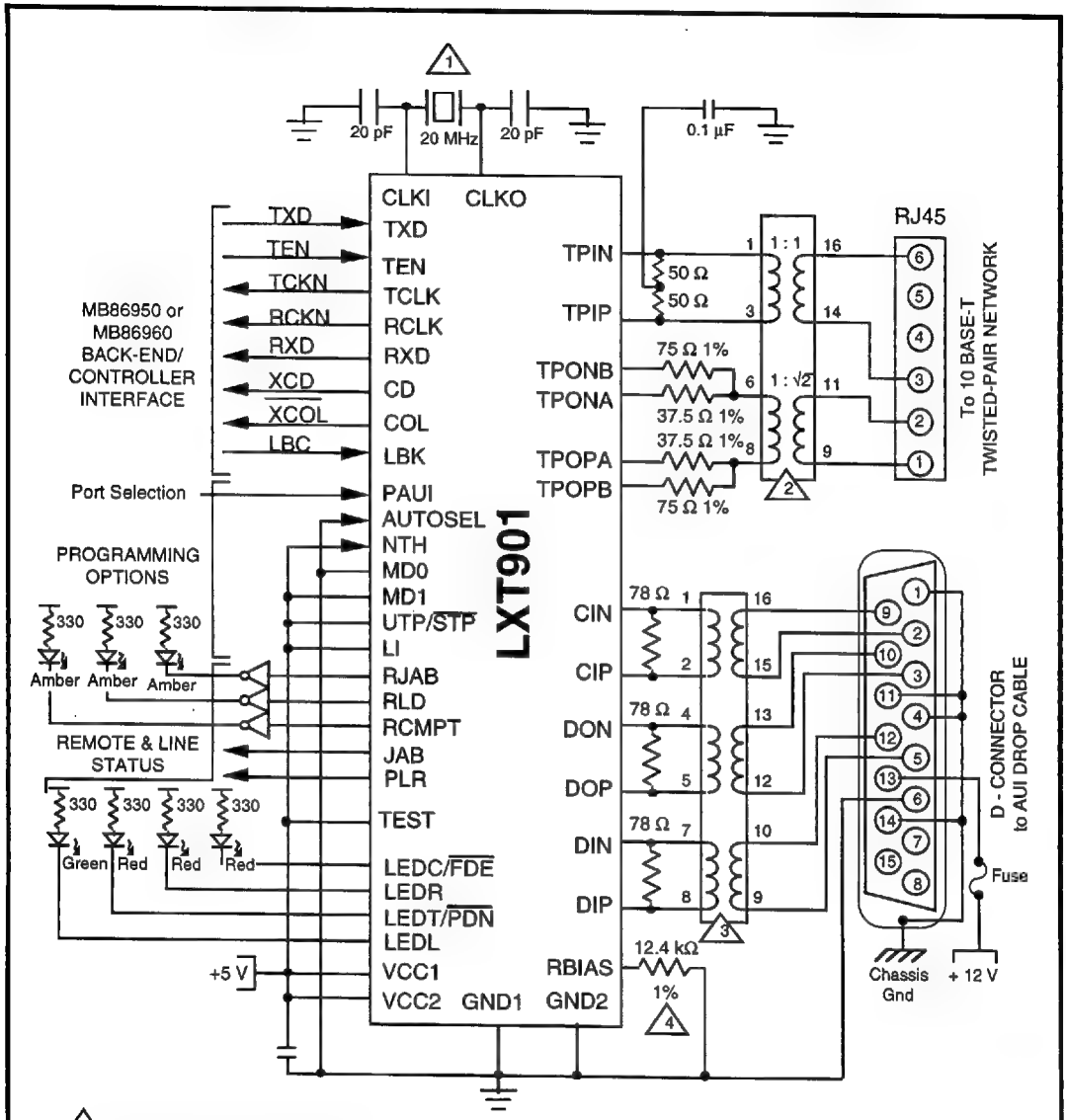
3. Bias resistor RBIAS should be located close to the pin and isolated from other signals.
4. Additional magnetics and switching logic (not shown) is required to implement the dual network solution.

Figure 10: LAN Adapter Board - Manual Port Select with Link Test Function



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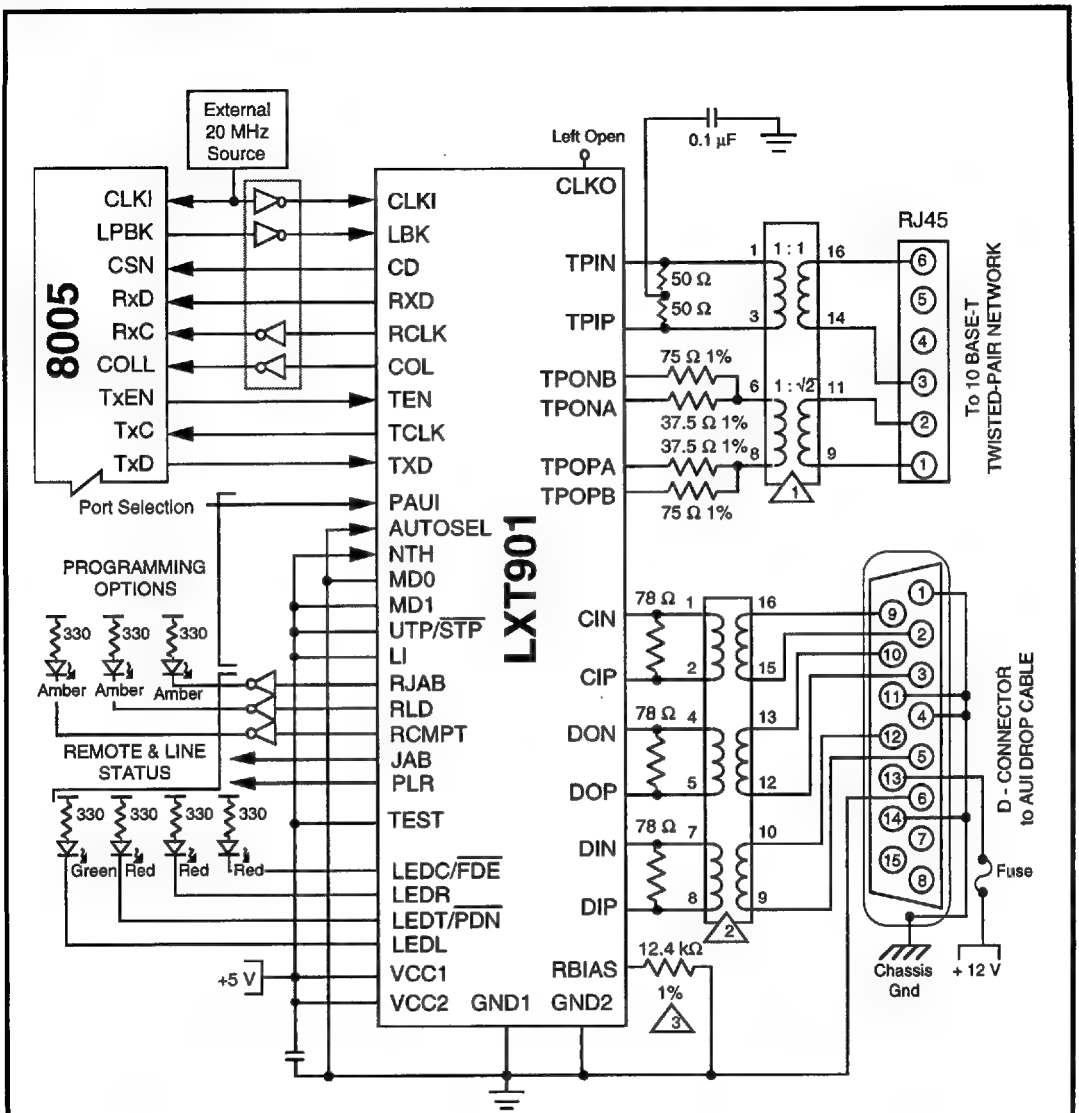
3. Suitable AUI transformers include the Fil-Mag 23Z90 and 23Z90SM; Valor LT6030 and ST7030; and Halo Electronics TD01-0756K and TG01-0756W.
4. Bias resistor RBIAS should be located close to the pin and isolated from other signals.

Figure 11: Manual Port Select with Seeq 8005 Controller



1 Suitable TP transformers include the Fil-Mag 23Z128, and 23Z128SM; Valor PT4069 and ST7011; Belfuse S553-0716 and A553-0716; and HALO Electronics TD42-2006Q and TG42-2006WH1.

2 Suitable AUI transformers include the Fil-Mag 23Z90 and 23Z90SM; Valor LT6030 and ST7030; and HALO Electronics TD01-756K, and TG01-0756W.

3 Bias resistor RBIAS should be located close to the pin and isolated from other signals.

Figure 12: 150 Ω Shielded Twisted-Pair Only Application

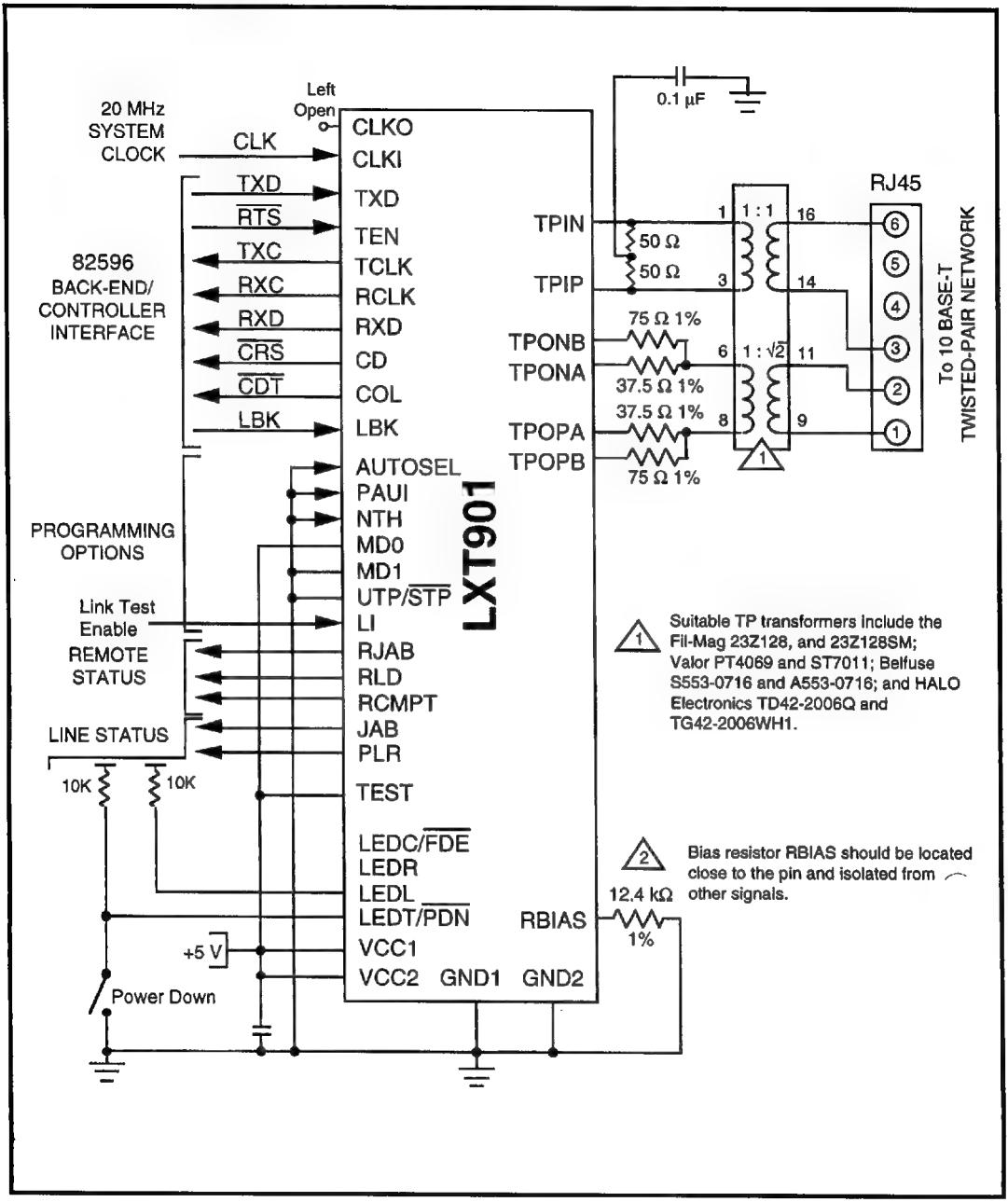
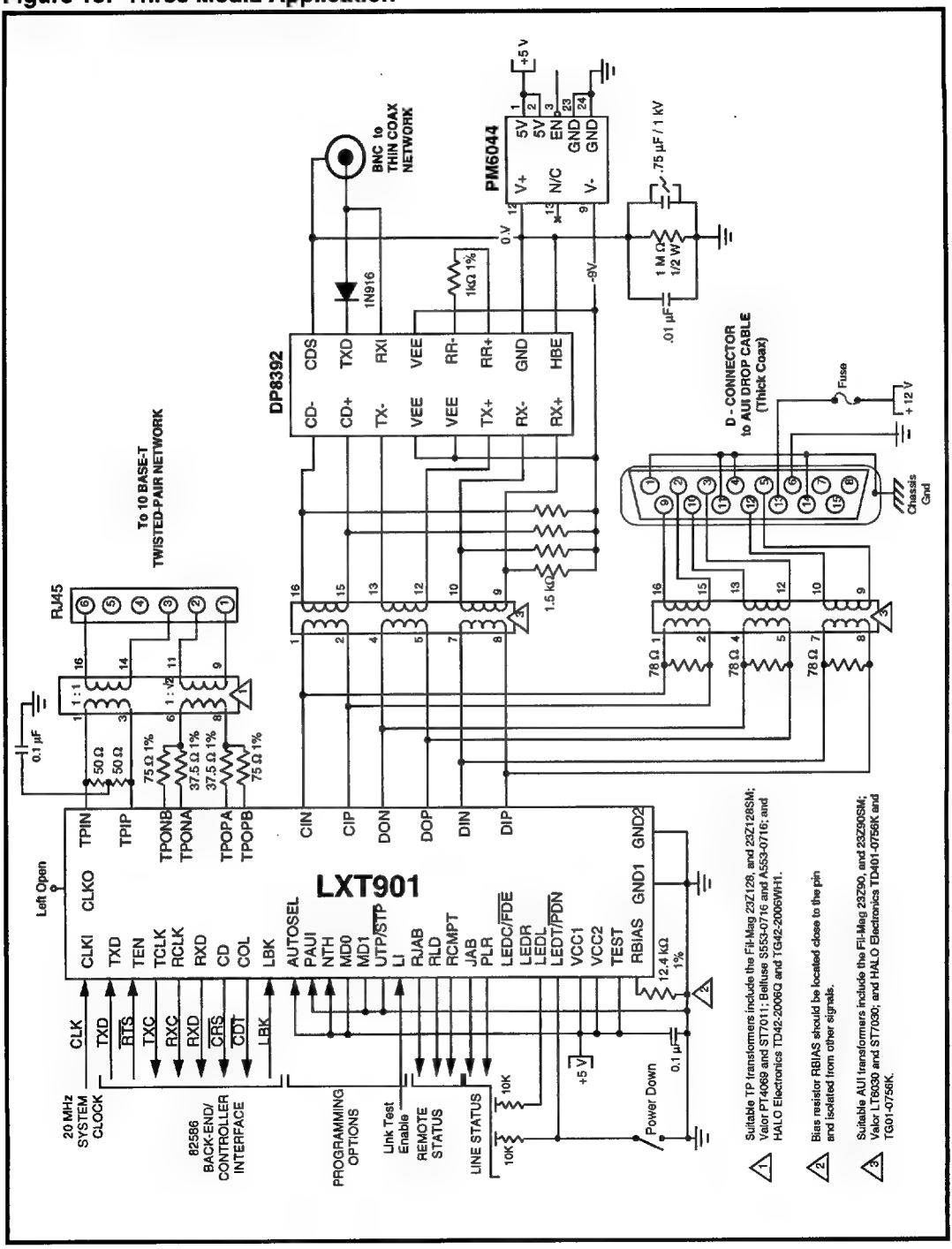


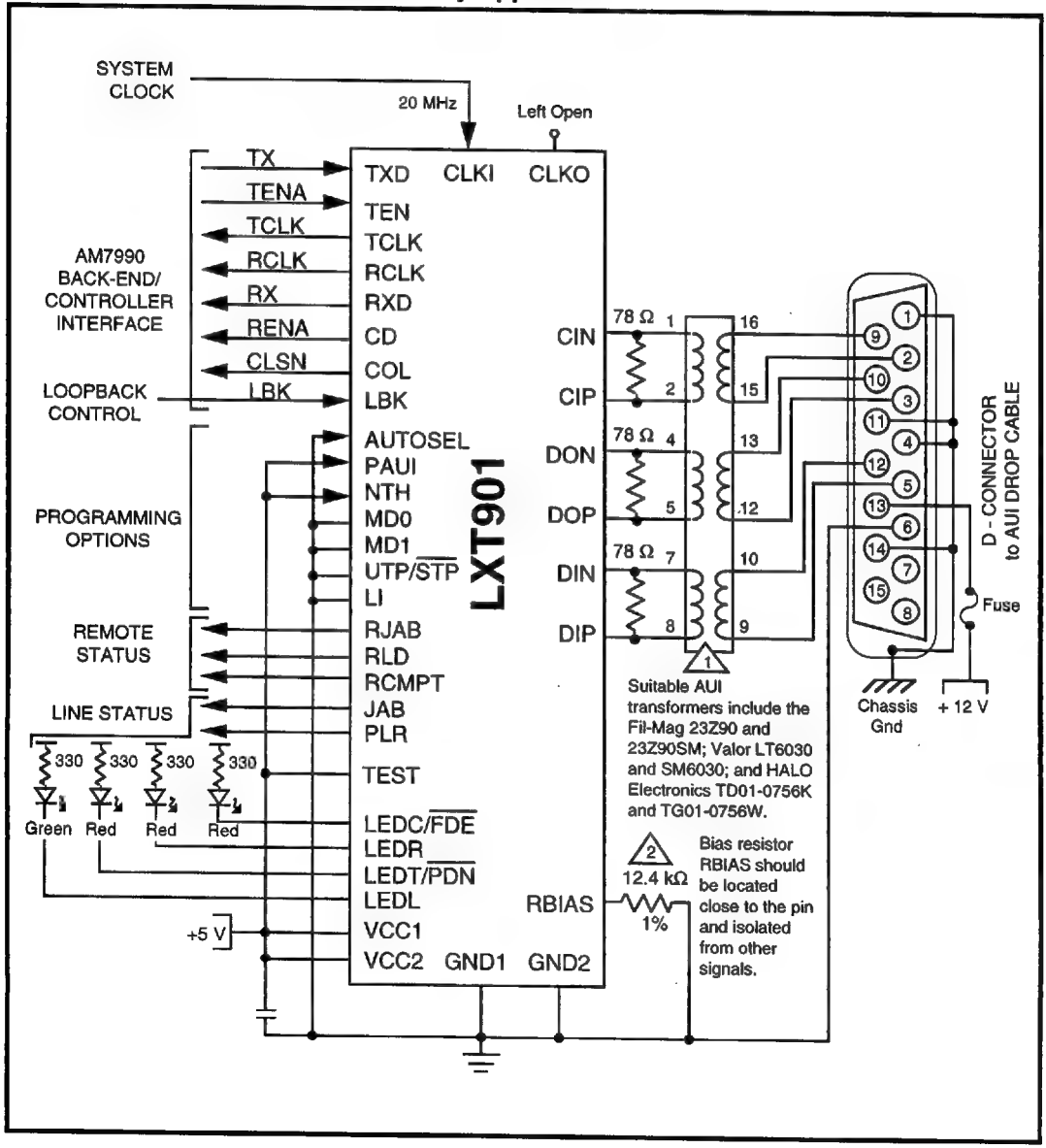
Figure 13: Three Media Application



AUI ENCODER/DECODER ONLY (FIGURE 14)

In this application the DTE is connected to a coaxial network through the AUI. AUTOSEL is tied Low and PAUI is tied High, manually selecting the AUI port. The twisted-pair port is not used. With MD1 and MD0 both Low, the LXT901 logic and framing are set to Mode 1 (compatible with AMD AM7990 controllers). The LI pin is tied Low, disabling the link test function. The LBK input controls loopback. A 20 MHz system clock is supplied at CLKI with CLKO left open.

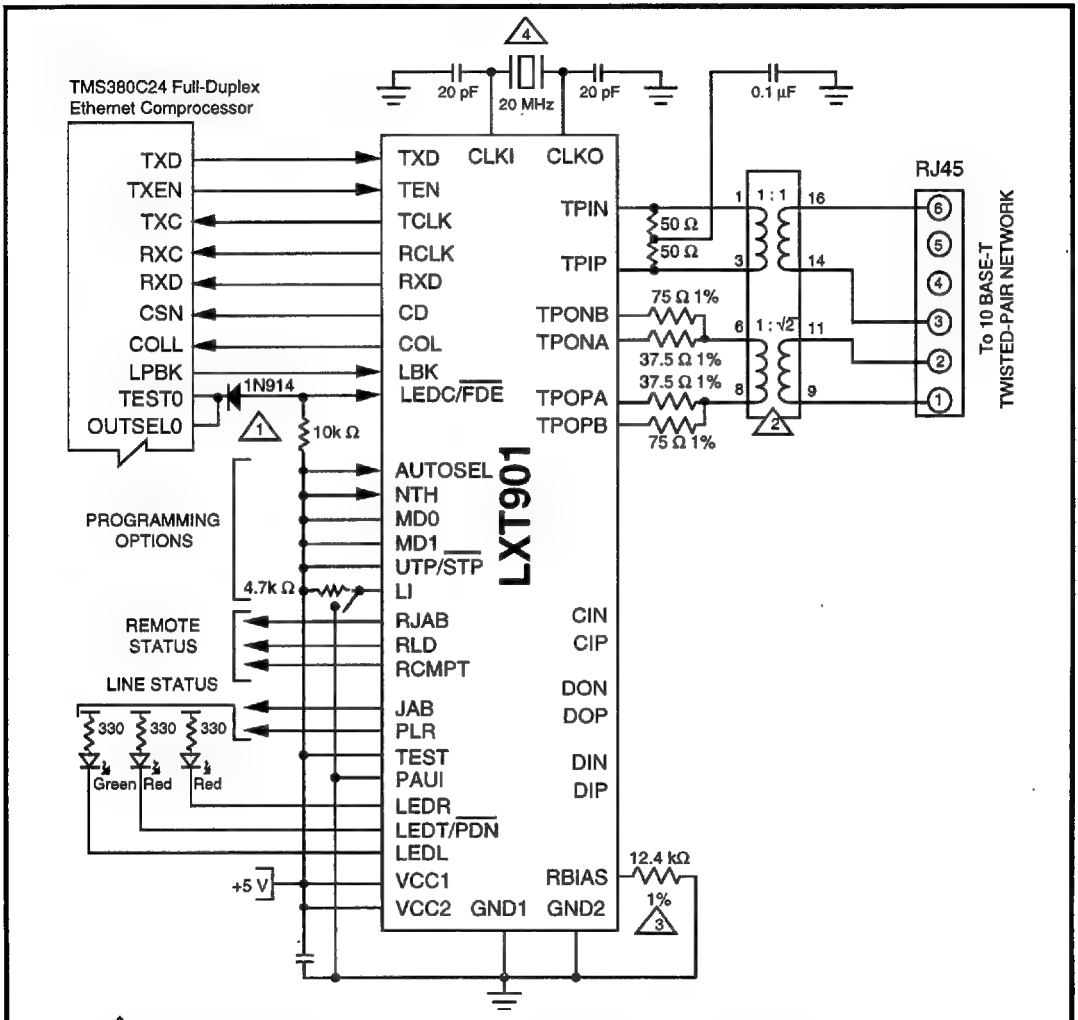
Figure 14: AUI Encoder/Decoder Only Application



FULL DUPLEX SUPPORT (FIGURE 15)

Figure 15 shows the LXT901 with a Texas Instruments 380C24 CommProcessor. The 380C24 is compatible with Mode 4 (MD0 and MD1 both High). When used with the 380C24 or other full duplex-capable controller, the LXT901 supports full-duplex Ethernet, effectively doubling the available bandwidth of the network. In this application the LXT901 AUI port is not used.

Figure 15: Full-Duplex Application



1. Half/Full Duplex Selection controlled by TMS380C24 pins TEST0 and OUTSEL0.
2. Suitable TP transformers include the Fil-Mag 23Z128, and 23Z128SM; Valor PT4069 and ST7011; Belfuse S553-0716 and A553-0716; and HALO Electronics TD42-2006Q and TG42-2006WH1.
3. Bias resistor RBIAS should be located close to the pin and isolated from other signals.
4. Suitable crystals include the MTRON MP-1 and MP-2.

TEST SPECIFICATIONS

NOTE

Minimum and maximum values in Tables 3 through 12 and Figures 16 through 39 represent the performance specifications of the LXT901 and are guaranteed by test except, as noted, by design.

Table 3: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	V_{CC}	–0.3	6.0	V
Ambient operating temperature	T_A	0	75	°C
Storage temperature	T_{STG}	-65	150	°C

CAUTION

Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed at these extremes.

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage [1]	V_{CC}	4.75	5.0	5.25	V	
Recommended operating temperature	T_{OP}	0	-	70	°C	

1. Voltage with respect to ground unless otherwise specified.

Table 5: I/O Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage [2]		V_{IL}	–	–	0.8	V	
Input High voltage [2]		V_{IH}	2.0	–	–	V	
Output Low voltage		V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output Low voltage		V_{OL}	–	–	10	% V_{CC}	I_{OL} < 10 µA
Output Low voltage (Open drain LED Driver)		V_{OLL}	–	–	0.7	V	I_{OLL} = 10 mA
Output High voltage		V_{OH}	2.4	–	–	V	I_{OH} = 40 µA
Output High voltage		V_{OH}	90	–	–	% V_{CC}	I_{OH} < 10 µA
Output rise time	CMOS	_	–	3	12	ns	C_{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	8	ns	
Output fall time	CMOS	–	–	3	12	ns	C_{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	8	ns	
CLKI rise time (externally driven)		–	–	–	10	ns	
CLKI duty cycle (externally driven)		–	–	50/50	40/60	%	
Supply Current	Normal mode	I_{CC}	–	65	85	mA	Idle Mode
		I_{CC}	–	90	110	mA	Transmitting on TP
		I_{CC}	–	70	90	mA	Transmitting on AUI
	Power Down Mode	I_{CC}	–	0.75	2	mA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 6: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	I_{IL}	–	–	-700	µA	
Input High current	I_{IH}	–	–	500	µA	
Differential output voltage	V_{OD}	± 550	–	± 1200	mV	
Differential squelch threshold	V_{DS}	150	220	350	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 7: TP Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Transmit timing jitter addition [2]	–	–	± 6.4	± 10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections [2,3]	–	–	± 3.5	± 5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN, CIP/CIN & DIP/DIN
Differential squelch threshold (Normal threshold : NTH = 1)	V_{DS}	300	420	585	mV	5 MHz square wave input
Differential squelch threshold (Reduced threshold : NTH = 0)	V_{DS}	180	250	345	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 8: Switching Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ	Max	Units
Jabber Timing:					
Maximum transmit time	–	20	–	150	ms
Unjab time	–	250	–	750	ms
Link Integrity Timing:					
Time link loss receive	–	50	–	150	ms
Link Min receive	–	2	–	7	ms
Link Max receive	–	50	–	150	ms
Link Transmit period	–	8	10	24	ms

Table 9: RCLK/Start-of-Frame Timing (Over Recommended Range)

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time	AUI	t_{DATA}	–	900	1100	ns
	TP	t_{DATA}	–	1300	1500	ns
CD turn-on delay	AUI	t_{CD}	–	50	200	ns
	TP	t_{CD}	–	400	550	ns
Receive data setup from RCLK	Mode 1	t_{RDS}	60	70	–	ns
	Modes 2, 3 and 4	t_{RDS}	30	45	–	ns
Receive data hold from RCLK	Mode 1	t_{RDH}	10	20	–	ns
	Modes 2, 3 and 4	t_{RDH}	30	45	–	ns

Table 10: RCLK/End-of-Frame Timing (Over Recommended Range)

Parameter	Type	Symbol	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Minimum	t_{RC}	5	1	27	5	bt
Rcv data throughput delay	Maximum	t_{RD}	400	375	375	375	ns
CD turn off delay[2]	Maximum	t_{CDOFF}	500	475	475	475	ns
Receive block out after TEN off	Typical[1]	t_{IFG}	5	50	–	–	bt

2. CD Turnoff delay measured from middle of last bit, so timing specification is unaffected by the value of the last bit.

Table 11: Transmit Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
TEN setup from TCLK	t_{EHCH}	22	–	–	ns
TXD setup from TCLK	t_{DSCH}	22	–	–	ns
TEN hold after TCLK	t_{CHEL}	5	–	–	ns
TXD hold after TCLK	t_{CHDU}	5	–	–	ns
Transmit start-up delay - AUI	t_{STUD}	–	200	450	ns
Transmit start-up delay - TP	t_{STUD}	–	350	450	ns
Transmit through-put delay - AUI	t_{TPD}	–	–	300	ns
Transmit through-put delay - TP	t_{TPD}	–	338	350	ns

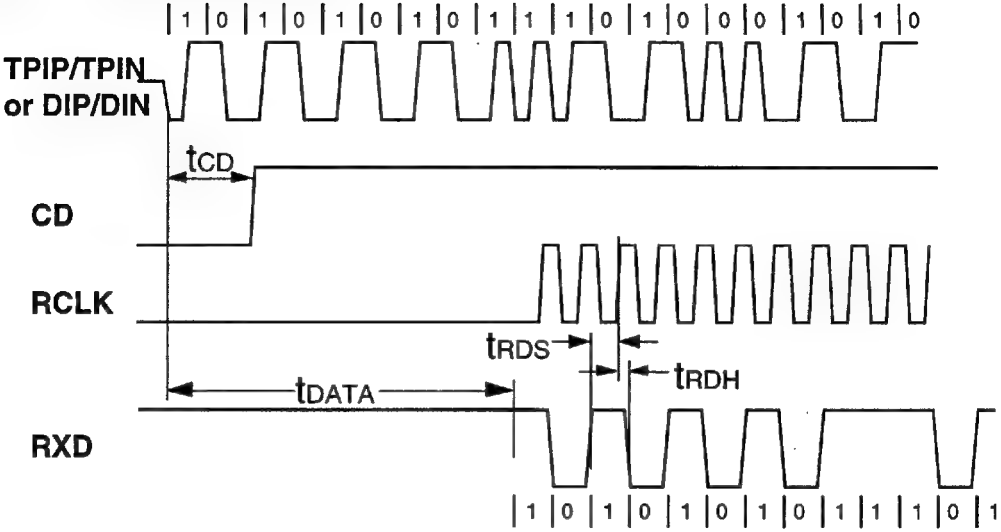
Table 12: Collision, COL/CI Output and Loopback Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL turn on delay	t_{COLD}	–	–	500	ns
COL turn off delay	t_{COLOFF}	–	–	500	ns
COL (SQE) Delay after TEN off	t_{SQED}	0.65	–	1.6	µs
COL (SQE) Pulse Duration	t_{SQEP}	500	–	1500	ns
LBK setup from TEN	t_{KHEH}	10	25	–	ns
LBK hold after TEN	t_{KHEL}	10	0	–	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

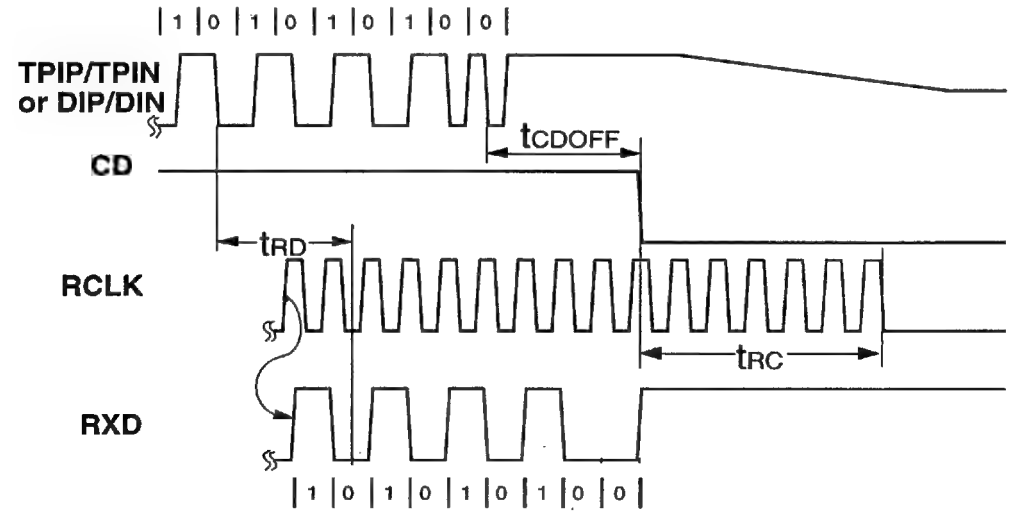
Figures 16 through 21 - Timing Diagrams for Mode 1 (MD1 = 0, MD0 = 0)

Figure 16: Mode 1 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes 25 ns after the rising edge of RCLK.

Figure 17: Mode 1 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes 25 ns after the rising edge of RCLK.

Figure 18: Mode 1 Transmit Timing

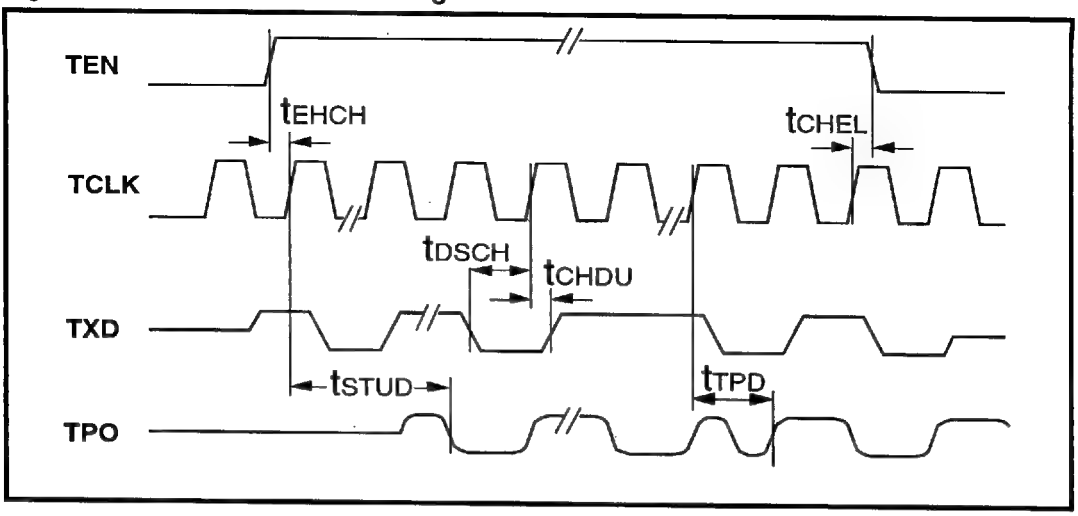


Figure 19: Mode 1 Collision Detect Timing

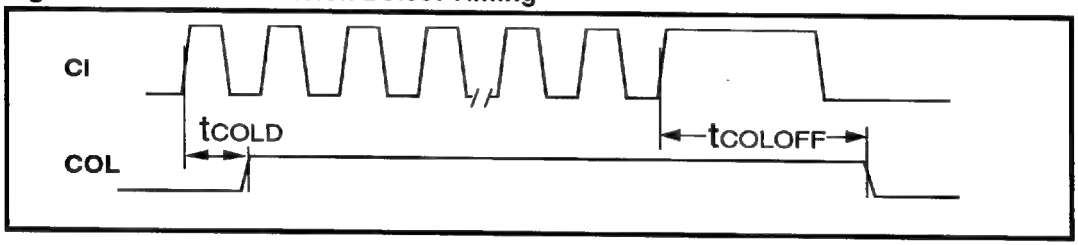


Figure 20: Mode 1 COL/CI Output Timing

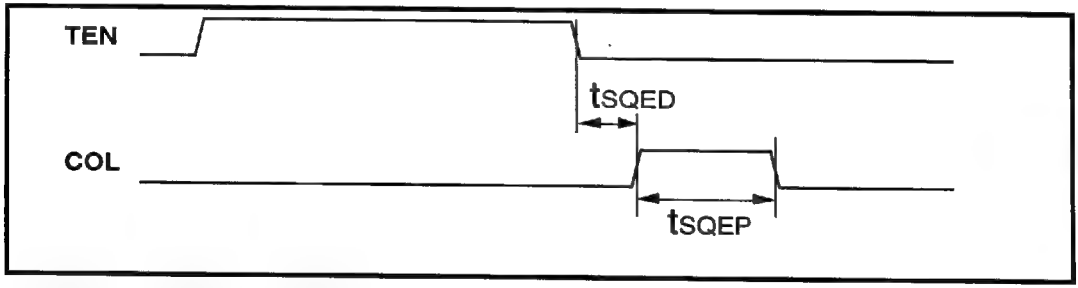
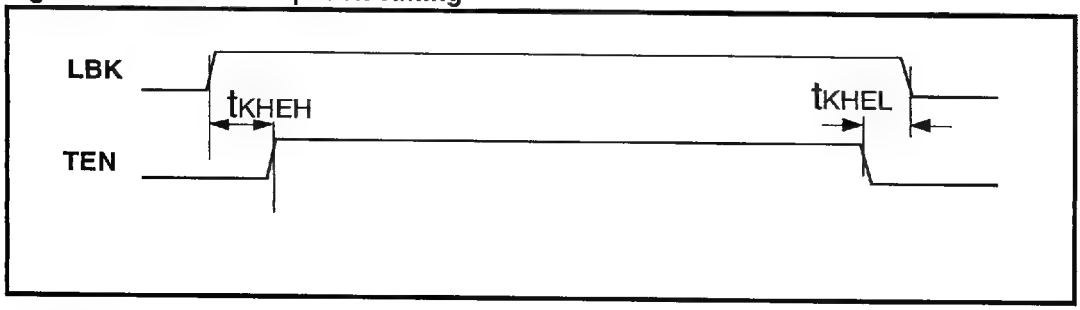
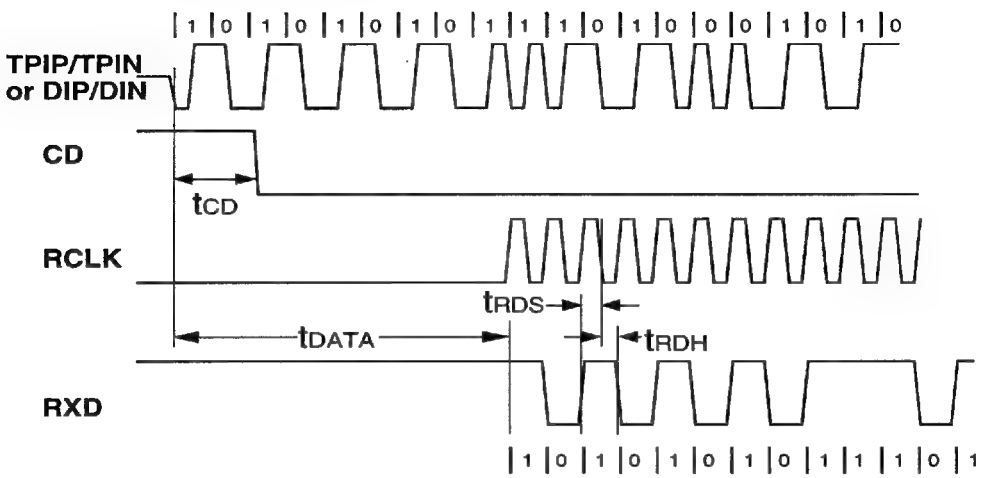


Figure 21: Mode 1 Loopback Timing



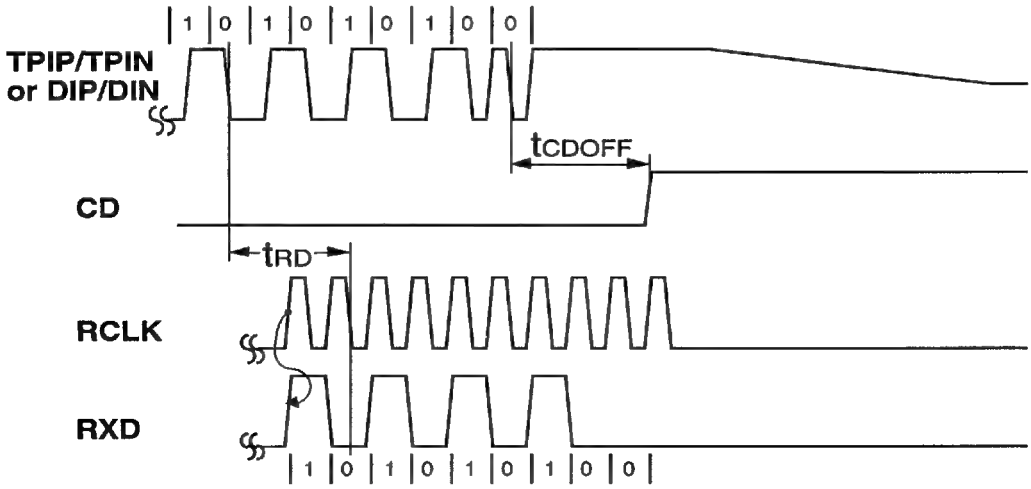
Figures 22 through 27 - Timing Diagrams for Mode 2 (MD1 = 0, MD0 = 1)

Figure 22: Mode 2 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 23: Mode 2 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 24: Mode 2 Transmit Timing

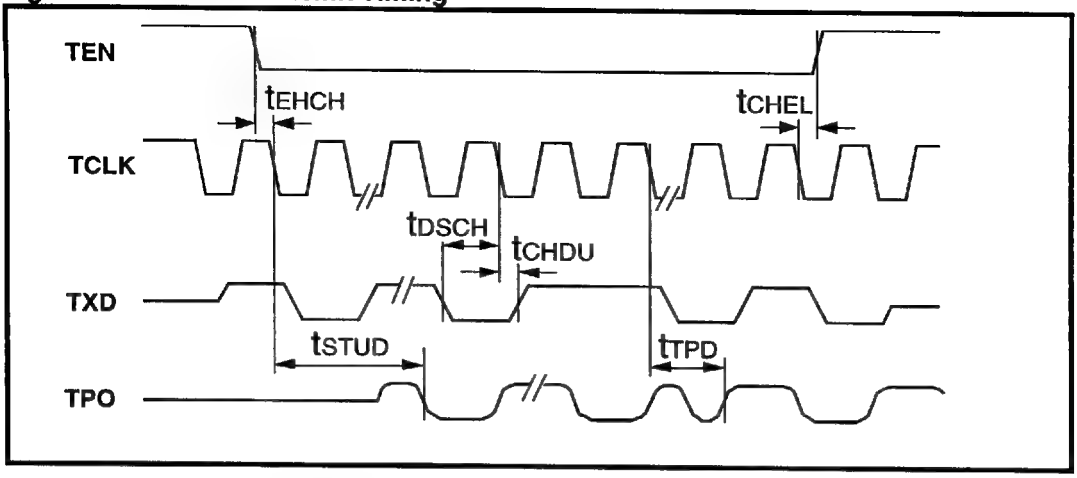


Figure 25: Mode 2 Collision Detect Timing

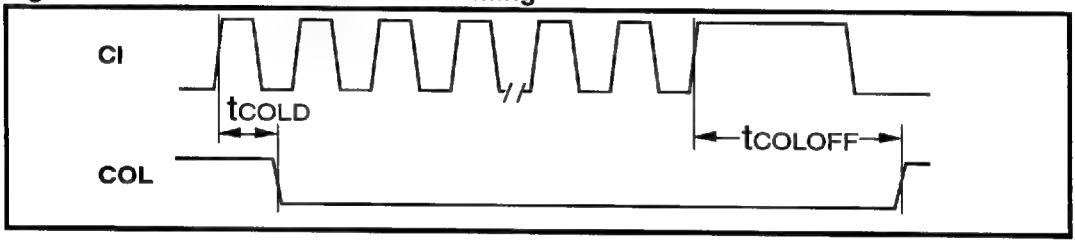
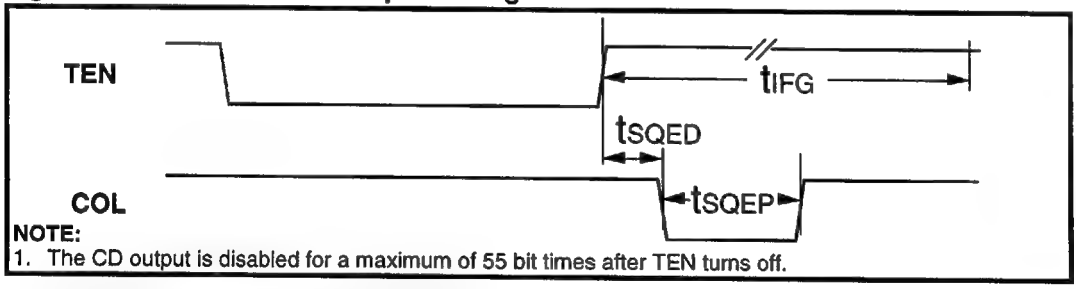
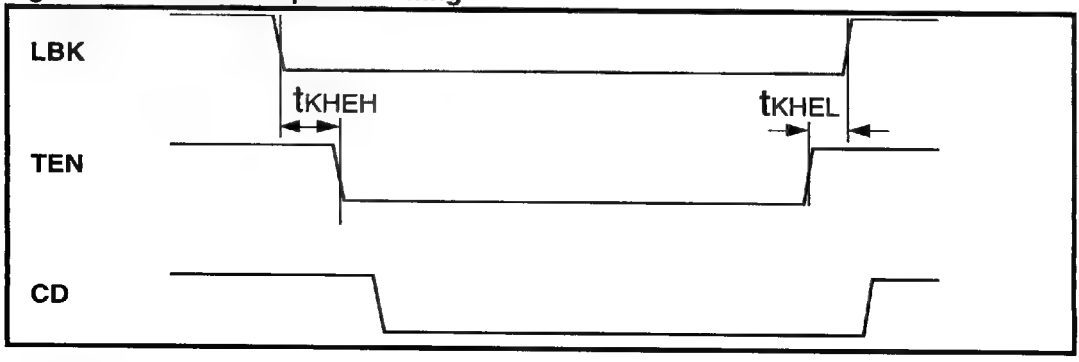


Figure 26: Mode 2 COL/CI Output Timing



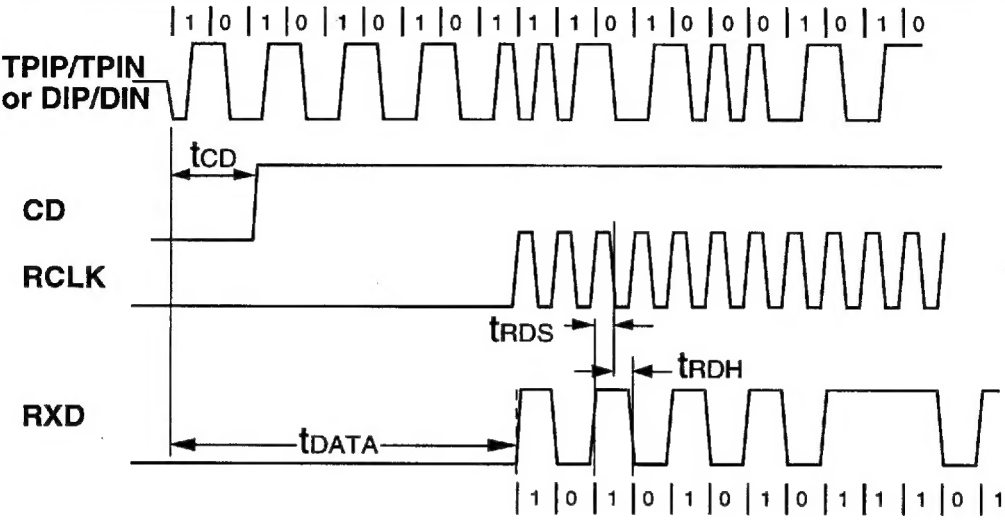
NOTE:
1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 27: Mode 2 Loopback Timing



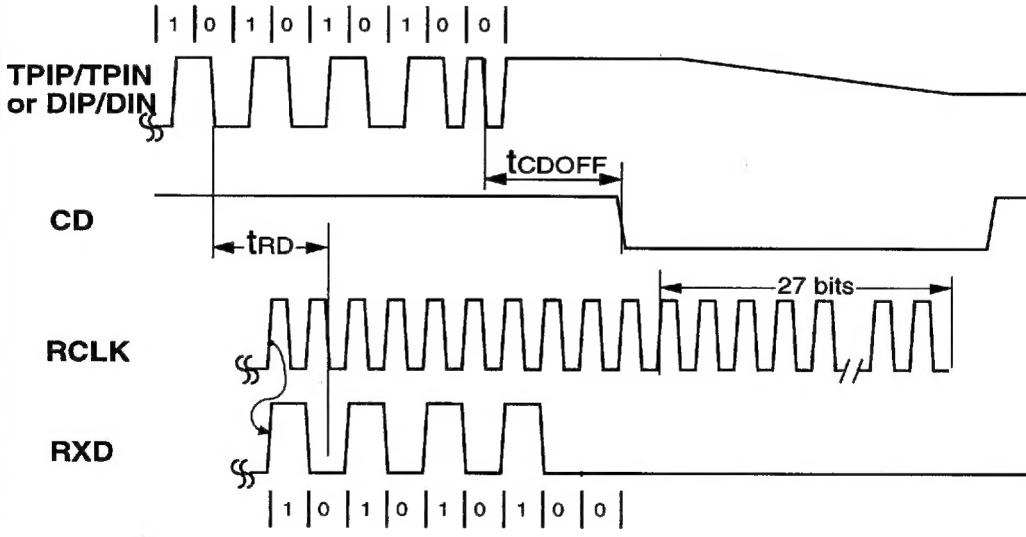
Figures 28 through 33 - Timing Diagrams for Mode 3 (MD1 = 1, MD0 = 0)

Figure 28: Mode 3 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 29: Mode 3 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 30: Mode 3 Transmit Timing

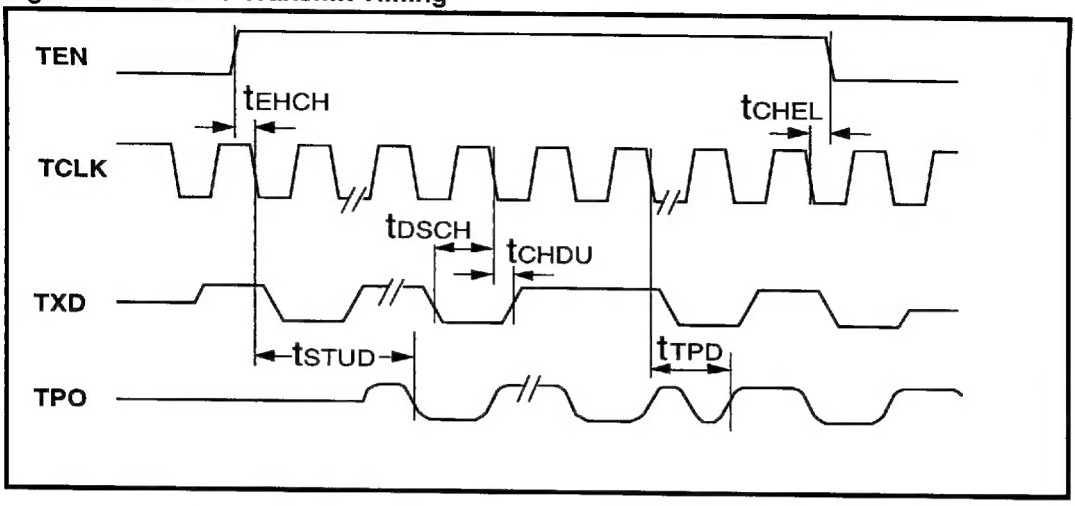


Figure 31: Mode 3 Collision Detect Timing

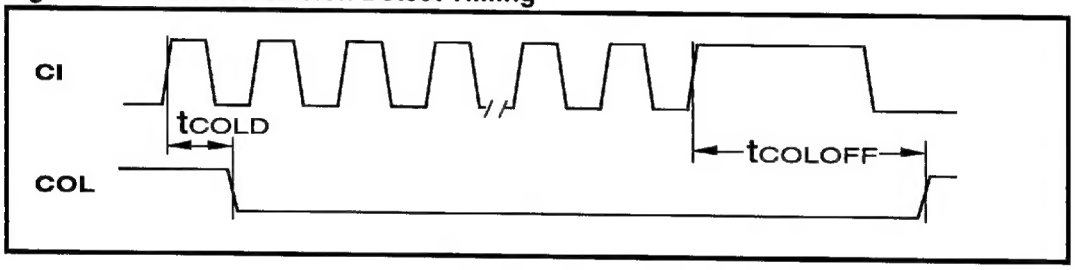


Figure 32: Mode 3 COL/CI Output Timing

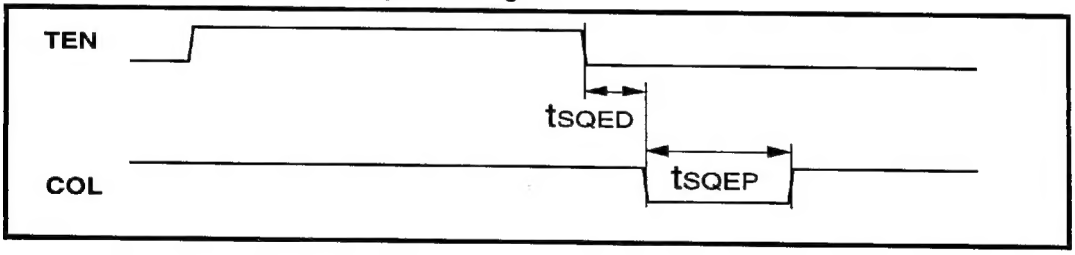
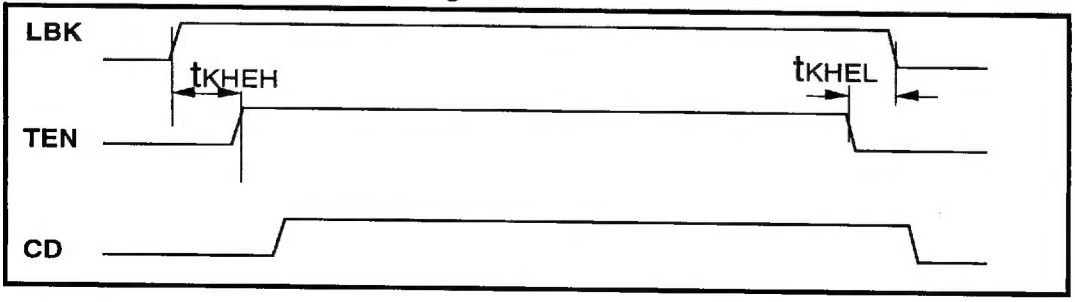
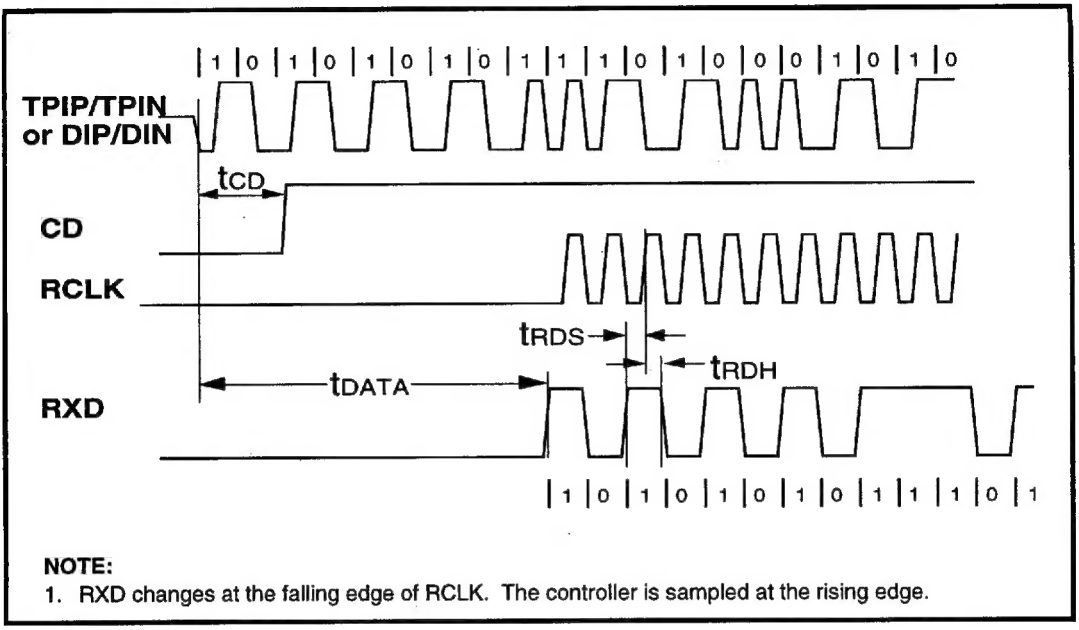


Figure 33: Mode 3 Loopback Timing



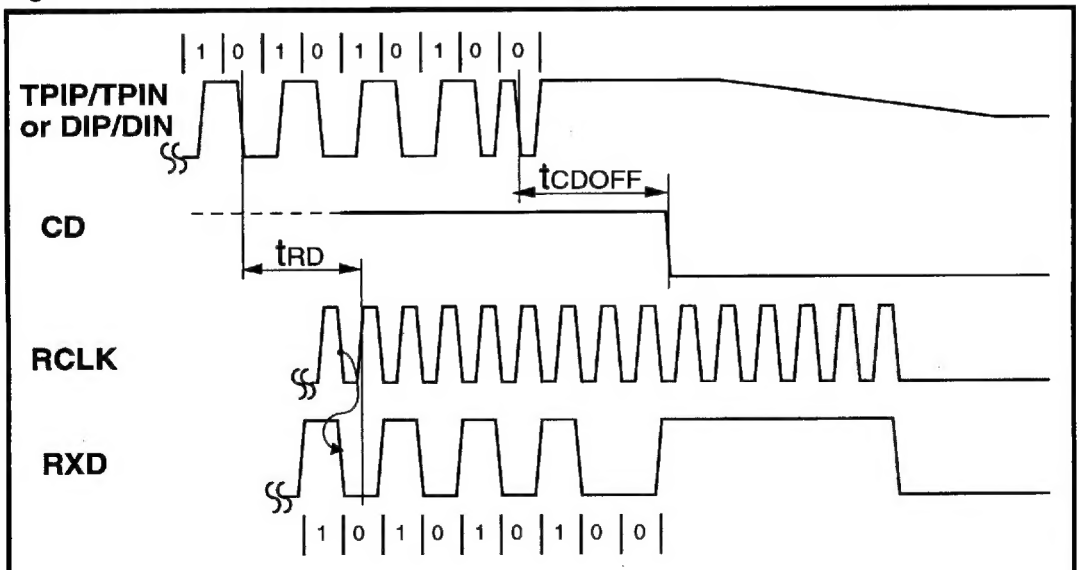
Figures 34 through 39 - Timing Diagrams for Mode 4 (MD1 = 1, MD0 = 1)

Figure 34: Mode 4 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 35: Mode 4 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 36: Mode 4 Transmit Timing

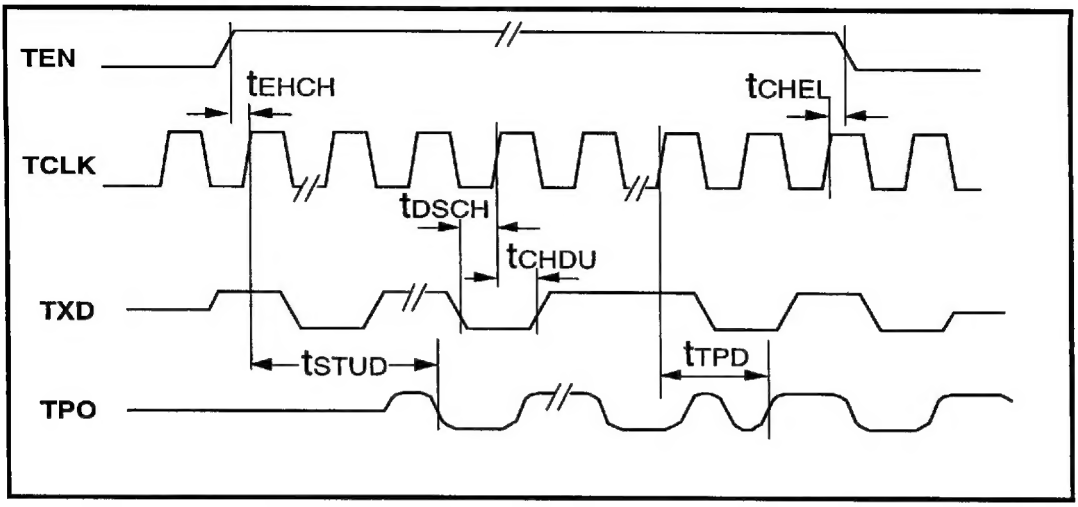


Figure 37: Mode 4 Collision Detect Timing

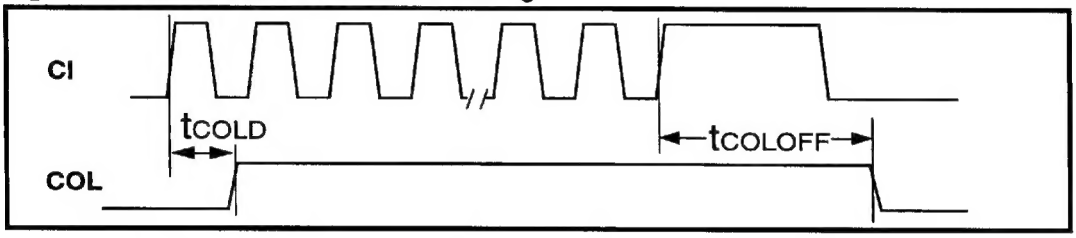


Figure 38: Mode 4 COL/CI Output Timing

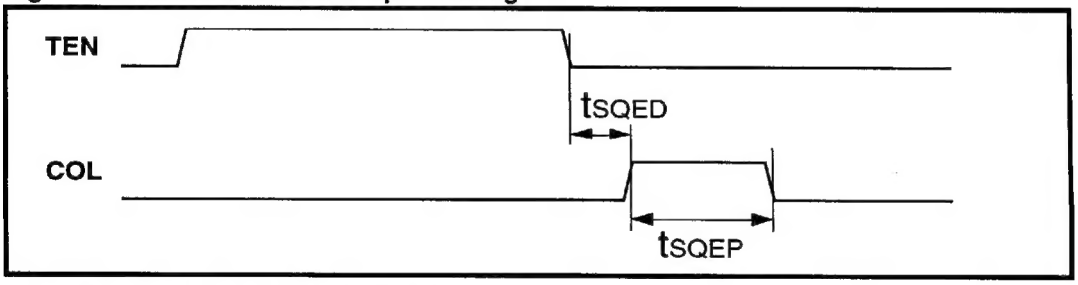


Figure 39: Mode 4 Loopback Timing